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Substitute for form 1449A/PTO				Complete If Known Application Number: 10/802,566 Filing Date: 03-17-2004 First Named Inventor: MOU-SHIUNG LIN Art Unit: 2892 Examiner Name: AJAY ARORA	
<b>INFORMATION DISCLOSURE          STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)					
Sheet	1	of	3	Attorney Docket No: 085027-0109	

### US PATENT DOCUMENTS

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	1	MISTRY, K. et al. "A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," IEEE International Electron Devices Meeting (2007) pgs. 247-250	
	2	EDELSTEIN, D.C., "Advantages of Copper Interconnects," Proceedings of the 12th International IEEE VLSI Multilevel Interconnection Conference (1995) pgs. 301-307	
	3	THENG, C. et al. "An Automated Tool Deployment for ESD (Electro-Static-Discharge) Correct-by-Construction Strategy in 90 nm Process," IEEE International Conference on Semiconductor Electronics (2004) pgs. 61-67	
	4	GAO, X. et al. "An improved electrostatic discharge protection structure for reducing triggering voltage and parasitic capacitance," Solid-State Electronics, 27 (2003), pgs. 1105-1110	
	5	YEOH, A. et al. "Copper Die Bumps (First Level Interconnect) and Low-K Dielectrics in 65nm High Volume Manufacturing," Electronic Components and Technology Conference (2006) pgs. 1611-1615	

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	6	HU, C-K. et al. "Copper-Polyimide Wiring Technology for VLSI Circuits," Materials Research Society Symposium Proceedings VLSI V (1990) pgs. 369-373	
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	11	VENKATESAN, S. et al. "A High Performance 1.8V, 0.20 µm CMOS Technology with Copper Metallization," Technical Digest IEEE International Electron Devices Meeting (1997) pgs. 769-772	
	12	JENEI, S. et al. "High Q Inductor Add-on Module in Thick Cu/SiLK™ single damascene," Proceedings from the IEEE International Interconnect Technology Conference (2001) pgs. 107-109	
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	14	SAKRAN, N. et al. "The Implementation of the 65nm Dual-Core 64b Merom Processor," IEEE International Solid-State Circuits Conference, Session 5, Microprocessors, 5.6 (2007) pgs. 106-107, pg. 590	
	15	KUMAR, R. et al. "A Family of 45nm IA Processors," IEEE International Solid-State Circuits Conference, Session 3, Microprocessor Technologies, 3.2 (2009) pgs. 58-59	
	16	BOHR, M. "The New Era of Scaling in an SoC World," International Solid-State Circuits Conference (2009) Presentation Slides 1-66	
	17	BOHR, M. "The New Era of Scaling in an SoC World," International Solid-State Circuits Conference (2009) pgs. 23-28	
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	20	MALONEY, T. et al. "Novel Clamp Circuits for IC Power Supply Protection," IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part C, Vol. 19, No. 3 (07-1996) pgs. 150-161	
	21	GEFFKEN, R. M. "An Overview of Polyimide Use in Integrated Circuits and Packaging," Proceedings of the Third International Symposium on Ultra Large Scale Integration Science and Technology (1991) pgs. 667-677	
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	25	LIN, M.S. et al. "A New System-on-a-Chip (SOC) Technology - High Q Post Passivation Inductors," Proceedings from the 53rd Electronic Components and Technology Conference (05-30-2003) pgs. 1503-1509	
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	28	LIN, M.S. et al. "A New IC Interconnection Scheme and Design Architecture for High Performance ICs at Very Low Fabrication Cost - Post Passivation Interconnection," Proceedings of the IEEE Custom Integrated Circuits Conference (09-24-2003) pgs. 533-536	

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